CLMPTO 01/10/05

CLAIMS 1-10 (CCANCELLED)

11. (previously presented) An integrated circuit arrangement comprising:

a semiconductor substrate having at least one doped region; and

a plane arranged on a surface of said semiconductor substrate and having a number of conductive useful structures and at least one conductive filler structure which exhibits essentially the same height, said conductive filler structure having no circuit-oriented function, said conductive filler structure being conductively connected to said doped region.

12. (previously presented) The integrated circuit arrangement according to claim 11, further comprising:

a planarizing insulation layer surrounding said conductive useful structures and said conductive filler structure; and

wherein said conductive useful structures and said conductive filler structure are essentially a same height.

CLAIMS 13-14 (CANCELLED)

15. (previously presented) The integrated circuit arrangement according to claim 11, wherein said conductive useful structures are gate electrodes; and wherein said conductive filler structure contains a material of said gate electrodes.

16. (previously presented) The integrated circuit arrangement according to claim 11, wherein said doped region is a doped well in said semiconductor substrate.

17. (previously presented) The integrated circuit arrangement according to claim 11, further comprising:

a metallization layer arranged above said plane wherein said conductive filler structure is arranged; and

a further contact connecting said conductive filler structure to said metallization layer.

18. (previously presented) A method for manufacturing an integrated circuit arrangement, said method comprising the steps of:

forming a doped region in a semiconductor substrate;

forming a plane on a surface of said semiconductor substrate by applying and structuring a conductive layer, said plane having a number of conductive useful structures and at least one conductive filler structure;

producing an insulation layer surrounding and covering said conductive useful structures and said conductive filler structure; and

producing a conductive connection between said conductive filler structure and said doped region.

CLAIM 19 (CANCELLED)

20. (previously presented) The method according to claim 18, further comprising the steps of:

producing a metallization layer above said plane wherein said conductive filler structure is formed; and

producing a further contact connecting said conductive filler structure to said metallization layer.

21. (previously presented) The integrated circuit arrangement according to claim 11,

wherein said doped region is said semiconductor substrate.

22. (previously presented) The integrated circuit arrangement according to claim 11, wherein the at least one conductive filler structure comprises:

a plurality of conductive filler structures that are arranged to establish a uniform geometrical occupation by the conductive useful structures and the conductive filler structures.

23. (previously presented) The method according to claim 18, wherein the conductive useful structures and the conductive filler structure exhibit essentially the same height, the conductive filler structure having no circuit-oriented function.

24. (previously presented) The method according to claim 18, wherein a plurality of conductive filler structures is provided, the conductive filler structures being arranged such that a uniform geometrical occupation by the conductive useful structures and the conductive filler structures is established.